a storage configured to store an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions in the plurality of instructions are included in the group of instructions, the data associated with the plurality of instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at a compile time; and

a switching circuit coupled to the storage, configured to issue the instructions in the group of instructions in parallel, to processing pipelines appropriate for the instructions in the group of instructions, in response to the data associated with the plurality of instructions.

92. (Amended) A method for issuing groups of instructions in parallel to processing pipelines, the method comprising:

storing in a storage, an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the at least another instruction to be issued at a time different from a time when the group of instructions is to be issued, the instruction frame also including data **[fields]** associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions are included in the group of instructions, the data associated with the instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at compile time; and

issuing the instructions in the group of instructions in parallel to processing pipelines appropriate for the instructions in the group of instructions, in response to the data associated with the plurality of instructions.

101. (Amended) A method of operating a microprocessor comprises:

compiling computer code to determine a frame of instructions;

storing in a memory storage the frame of instructions, the frame of instructions including a plurality of instructions and issue data, the plurality of instructions including at least a first instruction, a second instruction, and a third instruction, the issue data comprising data indicating that the first instruction is to be issued before the second instruction and the third instruction and that the second and third instructions are to be issued in parallel, and the issue data indicating respective processing units appropriate for the first instruction, the second instruction, and the third instruction; and

issuing the first instruction to a processing unit appropriate for the first instruction in response to the issue data; and

issuing the second instruction and the third instruction in parallel to respective processing units appropriate for the second instruction and the third instruction in response to the issue data.

-- 106. (New) A computing system having a plurality of processing pipelines for executing groups of individual instructions, within very long instruction words, each individual instruction to be executed in each group being executed by different processing pipelines in parallel, the computing system comprising:

a main memory for storing a very long instruction word;

a very long instruction word storage, coupled to the main memory, for receiving the very long instruction word from the main memory, and for holding the very long instruction word, the very long instruction word including a predetermined number N of individual instructions, and including at least one group of M individual instructions to be executed in parallel, where M<=N, each individual instruction in the very long instruction word storage to be executed having an a pipeline identifier indicative of a processing pipeline for executing the individual instruction, and having a group identifier indicative of a group of individual instructions to which the individual instruction is assigned for execution in parallel;

a group decoder responsive to the group identifier for each individual instruction in the very long instruction word storage to be executed for enabling each

individual instruction in the very long instruction word storage having a similar group identifier, to be executed in parallel by the plurality of processing pipelines; and

a pipeline decoder responsive to the pipeline identifier of each individual instructions in the very long instruction word storage to be executed for causing each individual instruction in a group of individual instructions having the similar group identifier to be supplied to the different processing pipelines.

107. (New) The computing system of claim 106 wherein M is greater than or equal to 1.

108. (New) The computing system of claim 106 wherein M is greater than 1.

109. (New) The computing system in claim 106, wherein the very long instruction word storage includes the at least one group of M individual instructions, and also includes group identifiers and pipeline identifiers for each individual instruction in the at least one group of M individual instructions.

110. (New) The computing system in claim 107, wherein each individual instruction in the at least one group of M individual instructions has associated therewith a different pipeline identifier.

111. (New) The computing system of claim 106, wherein the very long instruction word storage holds a first group of individual instructions to be executed in parallel and a second group of individual instructions to be executed in parallel after the first group, each individual instruction in the first group having associated therewith a first group identifier different from a second group identifier associated with each individual instruction in the second group, the first group and the second group being placed adjacent to each other in the very long instruction word storage.

112. (New) The computing system of claim 111 wherein:

the very long instruction word storage comprises a line in a cache memory having a fixed number of storage locations; and

the first group of individual instructions is placed at one end of the line in the cache memory, and the second group of individual instructions is placed next to the first group of individual instructions.

113. (New) A method of executing in a plurality of processing pipelines arbitrary numbers of instructions in a stream of instructions in parallel which have been compiled to determine which instructions can be executed in parallel, the method comprising:

in response to the compilation, assigning a common group identifier to a group of instructions which can be executed in parallel;

determining a processing pipeline for execution of each instruction in the group of instructions to be executed;

assigning a pipeline identifier to each instruction in the group;

associating the common group identifier and the pipeline identifier with the group of instructions;

forming a very long instruction word with a fixed number of the instructions including at least the group of instructions and the common group identifier as well as at least one other instruction having a different group identifier; and

storing the very long instruction word in a main memory.

114. (New) A method as in claim 113 further comprising:

placing the very long instruction word retrieved from the main memory into a very long instruction word register; and

executing the group of instructions in the plurality of processing pipelines in parallel.

115. (New) A method as in claim 114,

wherein the very long instruction word register holds at least two groups of instructions; and

wherein placing the instructions in the very long instruction word register comprises placing the group of instructions adjacent to the at least one other instruction having the different group identifier in the very long instruction word register.

116. (New) A method as in claim 115 wherein executing the group of instructions in parallel comprises:

coupling the very long instruction word register to a detection means to receive group identifiers associated with each instruction to be executed in the very long instruction word; and

supplying only instructions in the group of instructions to the processing pipelines in response to the group identifiers .

117. (New) In a computing system having a plurality of processing pipelines in which groups of individual instructions, within very long instruction words, are executable in parallel by processing pipelines, a method for supplying each individual instruction in a group to be executed in parallel to corresponding appropriate processing pipelines, the method comprising:

retrieving a very long instruction word from a main memory;

storing in a very long instruction word storage the very long instruction word, the very long instruction word including groups of individual instructions to be executed in parallel, the groups of individual instruction to be executed in the very long instruction word having associated therewith pipeline identifiers indicative of the corresponding appropriate processing pipeline which will execute the instructions and group identifiers indicative of groups of instructions;

using the group identifiers in the very long instruction word to identify an execution group; and

using the pipeline identifiers to execute each individual instruction in the execution group in the corresponding appropriate processing pipelines.

118. (New) In a computing system having a plurality of processing pipelines in which groups of individual instructions, from a very long instruction word, are executable in parallel by the plurality of processing pipelines, an apparatus for routing each individual instruction in a particular group to be executed in parallel to an appropriate processing pipeline, the apparatus comprising:

a main memory for storing the very long instruction word;

a very long instruction word storage coupled to the main memory, for receiving the very long instruction word from the main memory and for holding the very long instruction word, the very long instruction word including groups of individual instructions, individual instructions to be executed in the very long instruction word storage having associated therewith pipeline identifiers indicative of processing pipelines for executing the individual instructions and also having associated therewith group identifiers to designate groups of individual instructions to which individual instructions are assigned, the pipeline identifiers and the group identifiers included in the very long instruction word;

a switching circuit having a first set of connectors coupled to the very long instruction word storage and a second set of connectors coupled to the plurality of processing pipelines; and

a router coupled to the very long instruction word storage and the switching circuit, responsive to the pipeline identifiers for routing each individual instruction in a group of individual instructions from connectors of the first set of connectors onto appropriate connectors of the second set of connectors, to thereby supply each individual instruction in the group of individual instructions to be executed in parallel to the appropriate processing pipeline.

119. (New) The apparatus of claim 118,

wherein the first set of connectors includes a set of first communication buses, one first communication bus for each individual instruction to be executed in the very long instruction word storage;

wherein the second set of connectors includes a set of second communication buses, one second communication bus for each processing pipeline; and

wherein the router comprises:

a set of decoders coupled to the very long instruction word storage, the decoders in the set for receiving as input signals the pipeline identifiers included in the very long instruction word storage and in response thereto for supplying as output signals switch control signals corresponding to each individual instruction in the very long instruction word storage; and

a set of switches coupled to the set of decoders and to the switching circuit, one switch of the set of switches at each intersection of each of the first set of communication buses with each of the second set of communication buses, each switch for receiving the switch control signals and for providing connections in response to receiving a corresponding switch control signal to thereby supply each individual instruction in the group to be executed in parallel to the appropriate processing pipeline.

120. (New) The apparatus of claim 119 further comprising:

a detection circuit coupled to the very long instruction word storage, for receiving the group identifiers included in the very long instruction word storage to be executed and in response thereto supply a group control signal; and

wherein the set of decoders are also coupled to the detection circuit for receiving the group control signal and in response thereto supply the switch control signal for only those individual instructions in the group to be supplied to the plurality of processing pipelines.

121. (New) The apparatus of claim 120,

wherein the detection circuit comprises a multiplexer coupled to receive the group identifiers included in the very long instruction word storage and in response thereto allow the group of individual instructions to be supplied to the plurality of processing pipelines.

122. (New) Apparatus as in claim 121 wherein the multiplexer supplies output signals to the set of decoders to indicate the group of individual instructions to be next supplied to the plurality of processing pipelines.

123. (New) In a computing system having a plurality of processing pipelines in which groups of individual instructions, within a very long instruction word, are executable by the plurality of processing pipelines, individual instructions in the very long instruction word to be executed having associated therewith group identifiers and pipeline identifiers, an apparatus for routing each individual instruction of a group of individual instructions to be executed in parallel to an appropriate processing pipeline of the plurality of processing pipelines, the apparatus comprising;

a main memory for storing the very long instruction word;

a very long instruction word storage coupled to the main memory, for receiving the very long instruction word from the main memory and for holding the very long instruction word the very long instruction word including groups of instructions to be executed in parallel, including pipeline identifiers and group identifiers;

a selection circuit coupled to the very long instruction word storage for receiving the group identifiers included in the very long instruction word, for determining in response thereto a group of individual instructions to be executed in parallel, and for outputting a control signal;

a decoder circuit coupled to the selection circuit and to the very long instruction word storage, for receiving the control signal and the pipeline identifiers included in the very long instruction word, for determining in response thereto the appropriate processing pipeline for each individual instruction of the group, and for outputting switch control signals;

a switching circuit coupled to the decoder circuit , having a first set of connectors coupled to the very long instruction word storage for receiving the very long instruction word therefrom and a second set of connectors coupled to the plurality of processing pipelines, for coupling each individual instruction of the group to an appropriate processing pipeline in response to the switch control signals.

124. (New) The apparatus of claim 123,

wherein the first set of connectors comprises a set of first communication buses, one first communication bus for each individual instruction held in the very long instruction word storage;

wherein the second set of connectors comprises a set of second communication buses, one second communication bus for each processing pipeline;

wherein the decoder circuit comprises a set of decoders coupled to receive as first input signals the pipeline identifiers and as second input signals the pipeline identifiers; and

wherein the switching circuit comprises a set of switches, one switch for every intersection between each of the first set of connectors and each of the second set of connectors, each switch for providing connections, in response to receiving the switch control signals, between each individual instruction in the group to be executed in parallel to the appropriate processing pipeline.

125. (New) The apparatus of claim 124

wherein the selection means comprises a multiplexer coupled to receive the group identifiers for each individual instruction in the very long instruction word storage, and in response to the group identifiers, enable the decoder means to output switch control signals for each individual instructions of the group.

126. (New) The apparatus of claim 125,

wherein the multiplexer supplies a switch control signal to the decoder means to enable the decoder means to output switch control signals for each individual instruction of the group of individual instructions from the very long instruction word.

127. (New) In a computing system having a plurality of processing pipelines in which groups of individual instructions are executable, each individual instruction in a group executable in parallel by the plurality of processing pipelines, a method for transferring each individual instruction in a group to be executed through a switching unit having a first set of

connectors coupled to a very long instruction word storage for receiving individual instructions therefrom, a second set of connectors coupled to the plurality of processing pipelines, and switches between the first set and the second set of connectors, the method comprising:

retrieving the very long instruction word from a main memory;

storing in the very long instruction word storage, the very long instruction word, the very long instruction word having a set of individual instructions including at least one group of individual instructions to be executed in parallel, individual instructions in the at least one group having associated therewith pipeline identifiers indicative of the processing pipeline which will execute that individual instruction, the very long instruction word storage also including at least one other individual instruction not in the at least one group of individual instructions, the at least one other individual instruction also having associated therewith the pipeline identifiers; and

using the pipeline identifiers to control the switches between the first set of connectors and the second set of connectors to thereby supply each individual instruction in the at least one group to be executed in parallel to an appropriate processing pipeline.

128. (New) A method as in claim 127 wherein the step of using the pipeline identifiers comprises:

supplying the pipeline identifiers to individual decoders of a set of decoders, each decoder of which provides an output signal; and

using the output signals of the sets of decoders to control the switches between the first set of connectors and the second set of connectors to thereby supply each individual instruction in the at least one group to be executed in parallel to an appropriate processing pipeline.

129. (New) A method as in claim 128 wherein individual instructions in the storage further includes group identifiers associated therewith to designate among the instructions present in the very long instruction word storage, which of the individual instructions may be simultaneously supplied to the plurality of processing pipelines, and the method further comprises:

supplying a group of instructions to be executed by the processing pipelines together with the group identifiers to a selector;

using the group identifiers to provide output determination signals; and

using both the output determination signals and the output signals to control the switches between the first set of connectors and the second set of connectors to thereby supply each instruction in the at least one group to be executed in parallel to the appropriate processing pipeline.

130. (New) In a computing system having a plurality of processing pipelines in which groups of individual instructions are executable by the plurality of processing pipelines, a method for supplying each individual instruction in a group of individual instructions to be executed in parallel to an appropriate processing pipeline, the method comprising:

retrieving a very long instruction word from a main memory;

storing in a very long instruction word storage the very long instruction word retrieved from the main memory, the very long instruction word including groups of individual instructions to be executed in parallel, the individual instructions having associated therewith pipeline identifiers indicative of processing pipelines which will execute the individual instructions and having associated therewith group identifiers indicative of a group identification;

comparing the group identifiers to an execution group identifier of those instructions to be next executed in parallel; and

using the pipeline identifiers to control switches in a switch having a first set of connectors coupled to the very long instruction word storage for receiving the very long instruction word therefrom and a second set of connectors coupled to the plurality of processing pipelines to thereby supply each individual instruction in the at least one group to be executed in parallel to the appropriate processing pipeline. --